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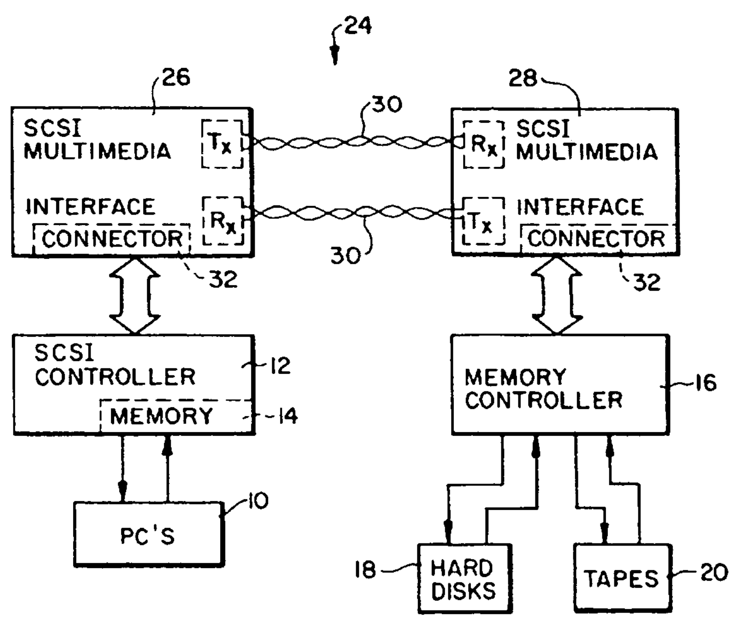
(54) Title: COMPUTER NETWORK EXTENDER



(57) Abstract

A network extender (24) for a computer network including multiple computers (10) interconnected with a shared, common memory (18, 20). A computer system interface (12) interconnects the multiple computers (10) and control data flow between the multiple computers (10) and a memory controller (16) connected to the memory (18, 20). First and second identical interfaces (26, 28) are respectively connected in data communication with the computer system interface (12) and the memory controller (16). Each interface (26, 28) includes a circuit for converting parallel data to serial data format and a circuit for converting serial data to parallel data format. The parallel to serial converting circuit and the serial to parallel converting circuit of the first interface (26) are respectively connected to the corresponding serial to parallel and the parallel to serial converting circuits of the second interface (28) by serial data communication conductors (30).

COMPUTER NETWORK EXTENDER

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates, in general, to computer networks, and more specifically, to interfaces for interconnecting multiple computers in a network configuration for access to common, stored programs and/or data stored in a memory.

Computer networks, such as a conventional prior art computer network shown in Fig. 1, typically include a number of computers, such as small or personal computers, which are interconnected via common data, address and control signal busses with a common memory comprising hard disks or tapes and shared peripheral I/O devices, such as CRTs and printers. Typically, a memory controller controls the flow of data and control signals between the busses and the memory and peripheral I/O devices.

An interface, such as a small computer system interface (SCSI), connects each peripheral computer to the shared busses to allow access of any individual computer to the common memory and I/O devices. The computer system interface controls the flow of data and control signals between the devices connected to the network.

However, in such computer networks, data communication between the peripheral computers, the computer system interface, the common memory and the peripheral I/O devices is in parallel bytes. Such parallel data transfer places a sever distance restriction on the network which limits the length of the communication busses between the computer system interface and the memory controller. Such

distances have been limited to less than 100 feet. Thus, the interface must be physically located in relatively close proximity to the memory, such as within 90 feet. This limits the use of computer networks to those applications where the computer system interface and the memory can be located in such close proximity.

Thus, it would be desirable to provide a computer network expander for a computer network which enables peripheral computers and computer system interfaces to be physically located at considerable distances from a common, shard memory and shared, peripheral I/O devices. It would also be desirable to provide a computer network expander which is simple and inexpensive to add to a computer network. Finally, it would be desirable to provide a computer network extender which does not require modification of the existing peripheral computers, computer system interface, memory or I/O devices.

SUMMARY OF THE INVENTION

The present invention is an extender for a computer network including multiple computers, a computer system interface interconnecting the multiple computers and controlling the flow of data to and from the computers, and a memory controller for controlling the flow of data to and from a common, shard memory. The computer network extender comprises a first interface connected in data communication with the computer system interface. A second, identical interface is connected in data communication with the memory controller or a second central processing unit.

Each of the first and second interfaces is identically constructed and includes a parallel to serial means for converting parallel data byte information to serial data format and serial to parallel means for converting serial data to parallel data byte format. The first and second interfaces also include means, responsive to the parallel to serial converting means, for transmitting serial data from the interface and means, associated with the serial to parallel converting means, for receiving serial data.

Serial data communication means connects the transmitting means of the first interface with the receiving means of the second interface and, also, connects the receiving means of the first interface with the transmitting means of the second interface for bi-directional serial data communication between the first and second interfaces. The serial communicating means may comprise any pair of data communication cables or conductors, such as a pair of twisted cables or fiber optical conductors.

The computer network extender of the present invention greatly extends the physical distance possible between a computer system interface and a memory controller or other processing unit in a computer network from the maximum of approximately 90 feet previously possible in computer networks utilizing parallel data transfer to a distance of up to 1.8 miles at 200 megabyte data transfer rates. The computer network extender includes an interface which is attachable to the computer system interface. The interface is simple and inexpensive in cost and requires no modification of the computer system interface or the

attached peripheral computers. An identical interface is attached to the memory and/or memory controller or other processing unit for receiving the signals from the first interface.

BRIEF DESCRIPTION OF THE DRAWINGS

The various features, advantages and other uses of the present invention will become more apparent by referring to the following detailed description and drawing in which:

FIG. 1 is a block diagram of a conventional, prior art computer network;

FIG. 2 is a block diagram of a computer network utilizing the computer network extender of the present invention;

FIGS. 3A and 3B are schematic diagrams of a portion of the computer network extender of the present invention showing the cable connectors and line drivers thereof;

FIGS. 4A and 4B are schematic diagrams of the parallel to serial data converting and transmitting means employed in the computer network extender of the present inventor; and

FIGS. 5A and 5B are schematic diagrams of the serial to parallel data converting and transmitting means employed in the computer network extender of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Throughout the following description and drawing, an identical reference number is used to refer to the same component shown in multiple figures of the drawing.

The present invention, as shown in the drawing, is a computer network extender for a computer network which increase the physical distance separating the computer system interface coupled to the peripheral computers and the main memory, memory controller or other processing unit. The computer network extender provides such increased distance by an interface which converts the parallel data from the computer system interface to serial format for high speed data transfer to the memory controller. An identical interface connected to the memory controller reconverts the serial data to parallel data format for use by the memory controller and common memory. This enables the distance between the small computer system interface and the memory controller or between any two data communication processing elements in a computer network to be up to 1.8 miles apart.

FIG. 2 depicts a block diagram of the computer network extender of the present invention employed in a conventional computer network. The elements of the computer network are illustrated in FIG. 1 and an identical reference number is used for the same elements in both figures.

The computer network may have any form and may contain any number of interconnected elements. Preferably, as shown in FIGS. 1 and 2, a typical computer network comprises a plurality of data processing devices 10, such as independent central processing units. Preferably, the central processing units 10 comprise small or personal computers. Such data processing units 10 are interconnected with a small computer system interface controller (SCSI) 12. The SCSI controller 12 includes an internal memory 14 which stores a

control program executed by the SCSI controller 12. The SCSI controller 12 controls the flow of data to and from the independent data processing units 10 and provides hierarchy, timing and signal access functions for the data processors 10.

A memory controller 16 also forms a part of a conventional computer network and controls the flow of data between the SCSI controller 12 and various memory devices, such as hard disks 18 and magnetic tape drives 20.

As shown in FIG. 1, the typical prior art computer network utilizes a common bus or buses 22 to provide data, address and control signal communication between the SCSI controller 12 and the memory controller 16. As is conventional, all data transfer between the individual data processing units 10 and the SCSI controller 12, the SCSI controller 12 and the memory controller 16 over the bus 22, and between the memory controller 16 and the hard disks 18 and the magnetic tape drives 20 is in parallel in which data bytes of 8, 16, etc. bit lengths are transferred simultaneously between the various portions of the network.

As shown in FIG. 2, the computer network extender 24 of the present invention includes first and second interfaces 26 and 28, respectively. The first interface 26 is disposed in data communication with the SCSI controller 12 or a first central processing unit; while the second interface 28 is disposed in parallel data communication with a second central processing unit, such as the memory controller 16. Serial data communication means in the form of pairs of two-wire conductors 30 interconnect the first and second interfaces 26 and 28 and provide high speed serial data transfer

between the first and second interfaces 26 and 28 as described hereafter.

Both of the first and second interfaces 26 and 28 provide parallel to serial data conversion to convert the parallel data from the respective SCSI controller 12 or memory controller 16 to a serial format for data transfer to the opposite interface over the serial data communication means 30. Such serial data is transferred in the interface to parallel format for data transfer with the respective central processing unit.

As each of the first and second interfaces 26 and 28 is identically constructed, the following discussion with reference to FIGS. 3A, 3B, 4A, 4B, 5A and 5B will be for the first interface 26; but is intended to apply to the construction of both of the first and second interfaces 26 and 28.

The interface 26 includes a connector 32, shown in FIG. 3A. The connector 32 provides single ended parallel data connection to the SCSI controller 12. The connector 32 provides various data connection labeled -DBϕ - DB8, as well as other negative signals labeled ATM, BSY, ASK, RST, MSG, SEL, C/D, REQ, I/O and ground required for conventional SCSI data transfer. A differential connector 32' is also provided in the interface 26 for differential data transfer with the SCSI controller 12 or the memory controller 16. This connector 32' provides the plus and minus data signals described above for each of the various data, address and control signals output or input to and from the SCSI controller 12 or the memory controller 16. The data terminals for pins in the connectors 32 and 32' are connected to individual transceivers 34, FIG. 3B. A separate transceiver 34

which provides bi-directional data signal receiving and transmitting functions is provided for each data signal terminal or pin on each of the connectors 32 and 32'. As the transceivers 34 are connected to the connectors 32 and 32' in the same manner, only a description of one transceiver 34 connection will be provided. It will be understood that similar circuit connections are provided for all of the signals on each of the connectors 32 and 32'.

The transceivers 34 may be any conventional bi-directional device, such as Model No. SN75176B. This is a conventional differential bus transceiver which may be employed in the present invention. A resistive biasing network is connected to and between the plus and minus inputs and plus and minus outputs of each transceiver 34 as shown in FIG. 3B.

The -DBφ signal from the connector 32 is connected to the negative input 36 of the transceiver 34 shown in FIG. 3B along with the -DBφ data signal from the connector 32'. Thus, the -DBφ signal is provided regardless of which connector 32 or 32' is employed in the interface 26 for connection to the SCSI controller 12. The +DBφ signal from the connector 32' is connected to the positive input 38 of the transceiver 34. Similar data connections are provided for all of the data signals on the connector 32 and the data signals on the connector 32' to each of the transceivers 34 thereby providing separate transceivers for each set of data signals and separate outputs therefrom. Each of the transceivers 34 outputs a pair of signals, such as signals labeled DIφA and $\overline{\text{DI}\phi\text{A}}$ for the first set of signals. Such signals are provided for each of the data signals on the

connectors 32 and 32' and are grouped in two separate data busses labeled DIAB and DOAB. Each of the signals on these data busses are connected to individual transceivers 34 as shown in FIG. 3B.

As shown in FIG. 4A, each interface, such as interface 26, includes means for converting the parallel data from the connectors 32 and 32' into serial data format. The parallel to serial data conversion means comprises three multiplexers 40, 42 and 44. Each of the multiplexers 40, 42, and 44 is a quad, dual input device which receives four input signals from either of two groups of signals under the control of a control signal labeled SEL. As shown in FIG. 4A, the first group of inputs to the multiplexer 40 comprise signals labeled DIϕA, DI1A, and DI2A and DI3A. Similarly, signals labeled DI4A, DI5A, DI6A, and DI7A is input to the multiplexer 44. Each of these signals is contained on the data bus labeled DIAB. The data signals labeled DIϕB-DI7B are input to an octal flip-flop 46 whose eight bit output is split into two groups respectively input to the multiplexers 40 and 42. The data signal DI8B is connected to a flip-flop 48. The output of the flip-flop 48 is connected as an input to the multiplexer 44. In this manner, an 18 bit word transferred in parallel from the SCSI controller 12 to the interface 26 passes through the connectors 32 or 32' and the transceivers 34 to the data bus DIAB. The multiplexers 40, 42 and 44 and the flip-flops 46 and 48 decode this data into two bytes of parallel data comprising a first 10 bit control signal byte followed by an 8 bit SCSI data byte.

The clock signals to the flip-flops 46 and 48, as well as the select signal SEL to the multiplexers 40, 42 and 44 are generated by an

oscillator 50 whose output is connected to a pair of serially connected flip-flops 52 and 54. The oscillator 50 and the flip-flops 52 and 54 provide proper timing signals so as to cascade and decode the data signals into the two byte words described above.

The output from the multiplexers 40, 42 and 44 is input in parallel to a taxi transmitter circuit 56. The taxi transmitter circuit is a parallel to serial data conversion device, such as one sold by Advanced Micro Devices as Model No. AM7968-125. The taxi transmitter circuit 58 converts the input parallel data to serial output data on positive and negative output lines 58 and 60, respectively. As shown in FIG. 4B, the outputs 58 and 60 are connected to a terminal 62 which is connected to one end of the serial communication means 30.

A similar circuit, shown in FIGS. 5A and 5B, is provided in the interface 26 for receiving serial data from the opposite interface 28 and converting such serial data to parallel data format for data transfer to the SCSI controller 12.

The serial communication means 30 conductors are connected to a receive data terminal 64, shown in FIG. 5B. A pair of positive and negative serial conductors 66 and 68, respectively, are connected between the terminal 64 and a taxi receive circuit 70, FIG. 5A. The taxi receive circuit 70 is a serial to parallel data conversion circuit sold by Advanced Micro Devices as Model No. AM7969-125. This taxi receive circuit 70 converts the serial input on lines 66 and 68 to nine bit parallel data output bytes. This output is divided

into two successive bytes with the first byte passing through octal flip-flops 72 and 74 to the data bus DOAB as data signals ~~DOØA-DO7A~~. The data signal ~~DO8A~~ is output from a pair of flip-flops 76 and 78 connected to the taxi receiver circuit 70. The second byte of data from the taxi receive circuit 70 is input through an octal flip-flop 80 to generate data signals ~~DOØB-DO6B~~. One output from the octal flip-flop 80 passes through flip-flop 82 to generate the signal labeled ~~DO7B~~. Another output from the octal flip-flop 80 passes through a flip-flop 84 to generate the signal ~~DO2B~~. A flip-flop 86 is directed connected to the taxi receive circuit 70 and generates data signal ~~DO8B~~. These signals are grouped and passed along the data bus DOAB to the transceivers 34, shown in FIG. 3B.

The output signals from the taxi transmit circuit 56 and the taxi receive circuit 70 are also connected to illumination means 90, shown in FIG. 5B, for indicating the receive, power on and transmit modes of operation of the interface 26.

As noted above, the serial data communication means 30 connected between the interfaces 26 and 28 connects the transmit terminal 62 in the first interface 26 to the receive data terminal 64 in the second interface 28. A second serial data communication means 30 connects transmit data terminal 62 in the second interface 28 with the receive data terminal 64 in the first interface 26. The signal data communication means 30 may comprise any two-wire electrical conductor, such as a twisted pair of twin fibers or twin coaxial cables. Alternately, fiber optic conductors may be employed along with appropriate transceiver drivers.

In operation, as shown in FIG. 2, output a signals from the SCSI controller 12 are output in parallel to the first interface 26. These signals are converted by the parallel to serial converting means shown in FIGS. 3A and 3B to serial format and transmitted over serial data communication cables 30 to the second interface 28. The second interface 28 reconverts the serial data to parallel format and transfer such data in parallel to the memory controller 16.

A reverse path from the memory controller 16 to the SCSI controller is also provided with the data being likewise converted from parallel to serial form and transmitted over the serial data communication cable 30 to the first interface 26 where it is again reconverted from serial to data format and transferred to the SCSI controller 12. This permits high speed serial data transfer between the first and second interfaces 26 and 28 over a considerable distance, such as up to 1.8 miles. This allows the SCSI controller 12 to be located at such a considerable distance from the memory controller 16 thereby providing increased flexibility and application of the computer network employing the computer network extender of the present invention. The computer network extender is of simple construction and requires no modification to conventional SCSI controllers, memory controllers and other memory devices.

WHAT IS CLAIMED IS:

1. In a data communication network formed of a first central processing unit connected to a plurality of peripheral central processing units and operating a stored control program for controlling data flow to and from the peripheral central processing units and a second central processing unit controlling data flow to and from a memory means under a stored control program, the improvement comprising:

a first interface connected in data communication with the first central processing unit;

a second interface connected in data communication with the second central processing unit;

each of the first and second interfaces comprising:

parallel to serial means for converting parallel data byte information to serial data format;

serial to parallel means for converting serial data to parallel data byte information;

means, responsive to the parallel to serial converting means, for transmitting serial data; and

means, associated with the serial to parallel converting means, for receiving serial data; and

serial data communication means for connecting the transmitting means of the first interface and the receiving means of the second interface and for connecting the receiving means of

the first interface and the transmitting means of the second interface in serial data communication.

2. The improvement of claim 1 further including:

connector means for connecting the first and second interfaces to the first and second central processing units for parallel data communicating therebetween; and

bi-directional transceiver means connected to each signal in the connector means.

3. The improvement of claim 2 further including:

multiplexer means for decoding parallel data from the transceiver means and inputting data to the parallel to serial converting means.

4. The improvement of claim 3 wherein the parallel data is 18 bits and the multiplexer means selects the parallel data in two successive parallel bytes.

5. The improvement of claim 1 wherein the serial data communication means comprises a pair of data communication conductors.

6. The improvement of claim 2 further including:

storage means, connected to the output of the serial to parallel converting means, for forming successive bytes of data output from the serial to parallel converting means;

the storage means being connected to the transceiver means.

7. A network extender for a data communication network having at least one data processing device and a memory means comprising:

a first interface connected in data communication with the first central processing unit;

a second interface connected in data communication with the second central processing unit;

each of the first and second interfaces comprising:

parallel to serial means for converting parallel data byte information to serial data format;

serial to parallel means for converting serial data to parallel data byte information;

means, responsive to the parallel to serial converting means, for transmitting serial data; and

means, associated with the serial to parallel converting means, for receiving serial data; and

serial data communication means for connecting the transmitting means of the first interface and the receiving means of the second interface and for connecting the receiving means of the first interface and the transmitting means of the second interface in serial data communication.

8. The network extender of claim 7 further including:

a plurality of data processing devices, the memory means being shared with each data processing device.

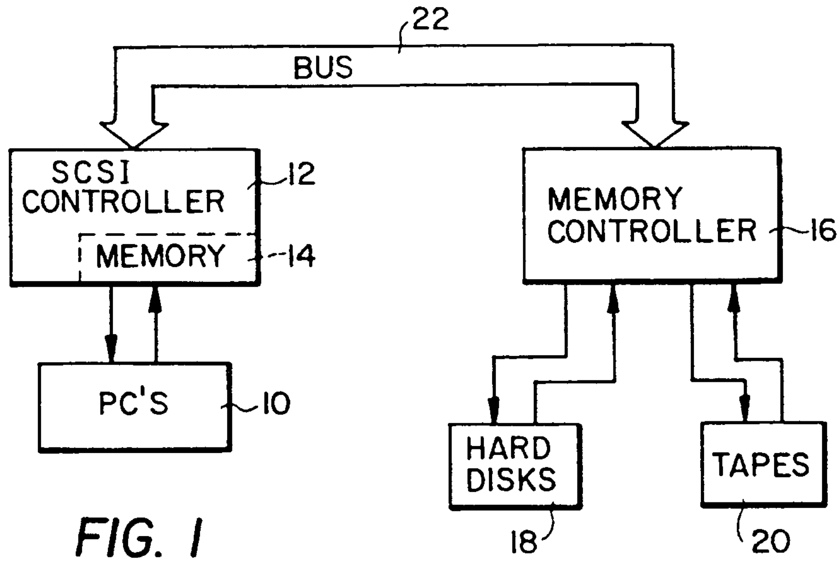
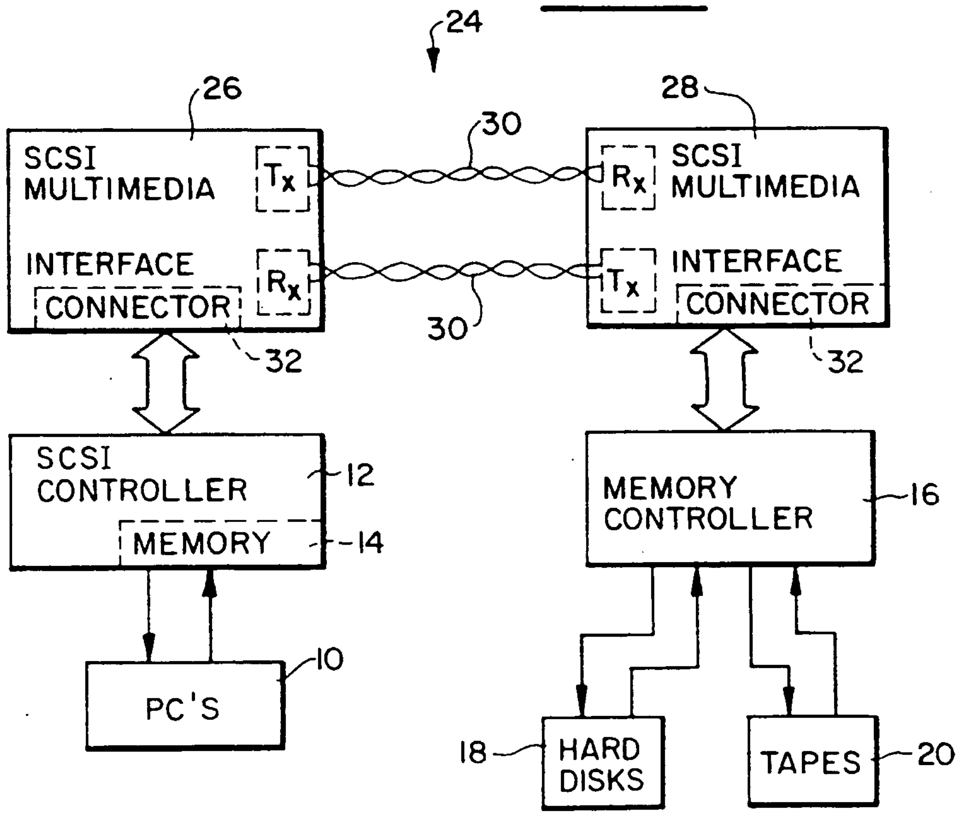


FIG. 1
(PRIOR ART)

FIG. 2



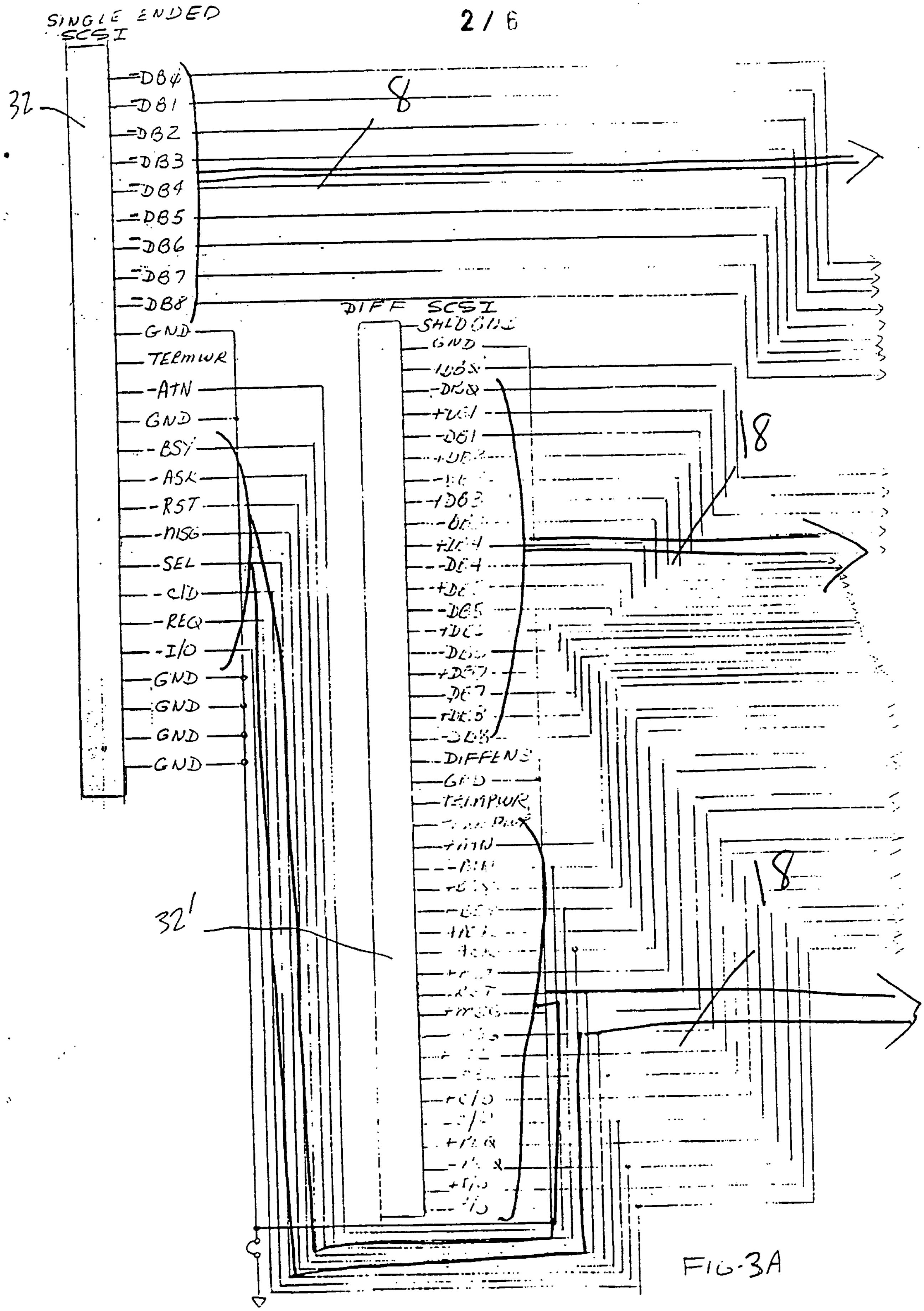

SINGLE ENDED SCSI
32
-DBφ
-DB1
-DB2
-DB3
-DB4
-DB5
-DB6
-DB7
-DB8
8
GND
TERMPWR
-ATN
GND
-BSY
-ASK
-RST
-MSG
-SEL
-C/D
-REQ
-I/O
GND
GND
GND
GND
DIFF SCSI
SHLD GND
GND
-DB1
18
+DB3
-DB4
-DB5
-DB7
DIFFSENS
TERMPWR
+C/D
18
32'

FIG-3A

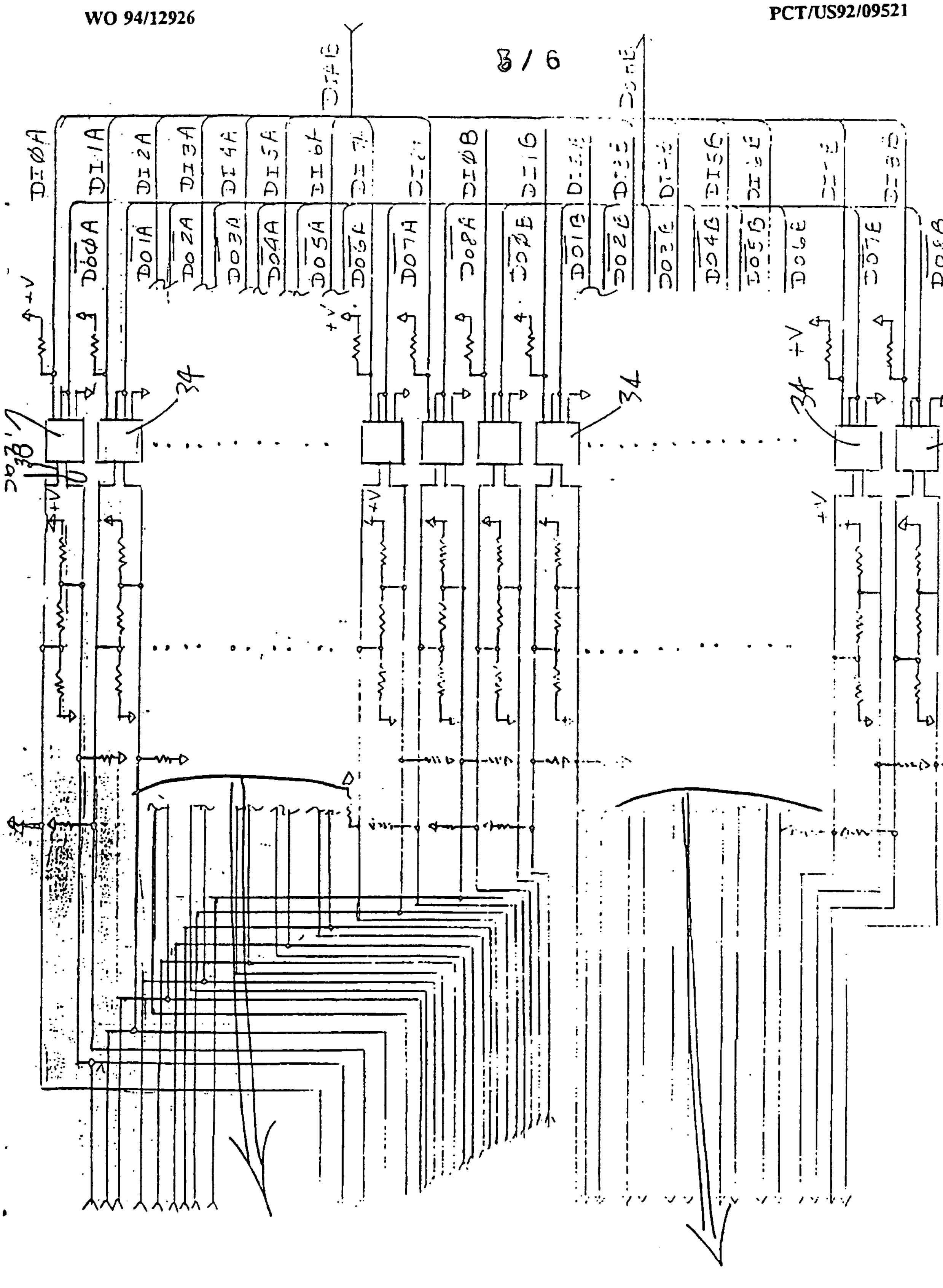


FIG. 3B

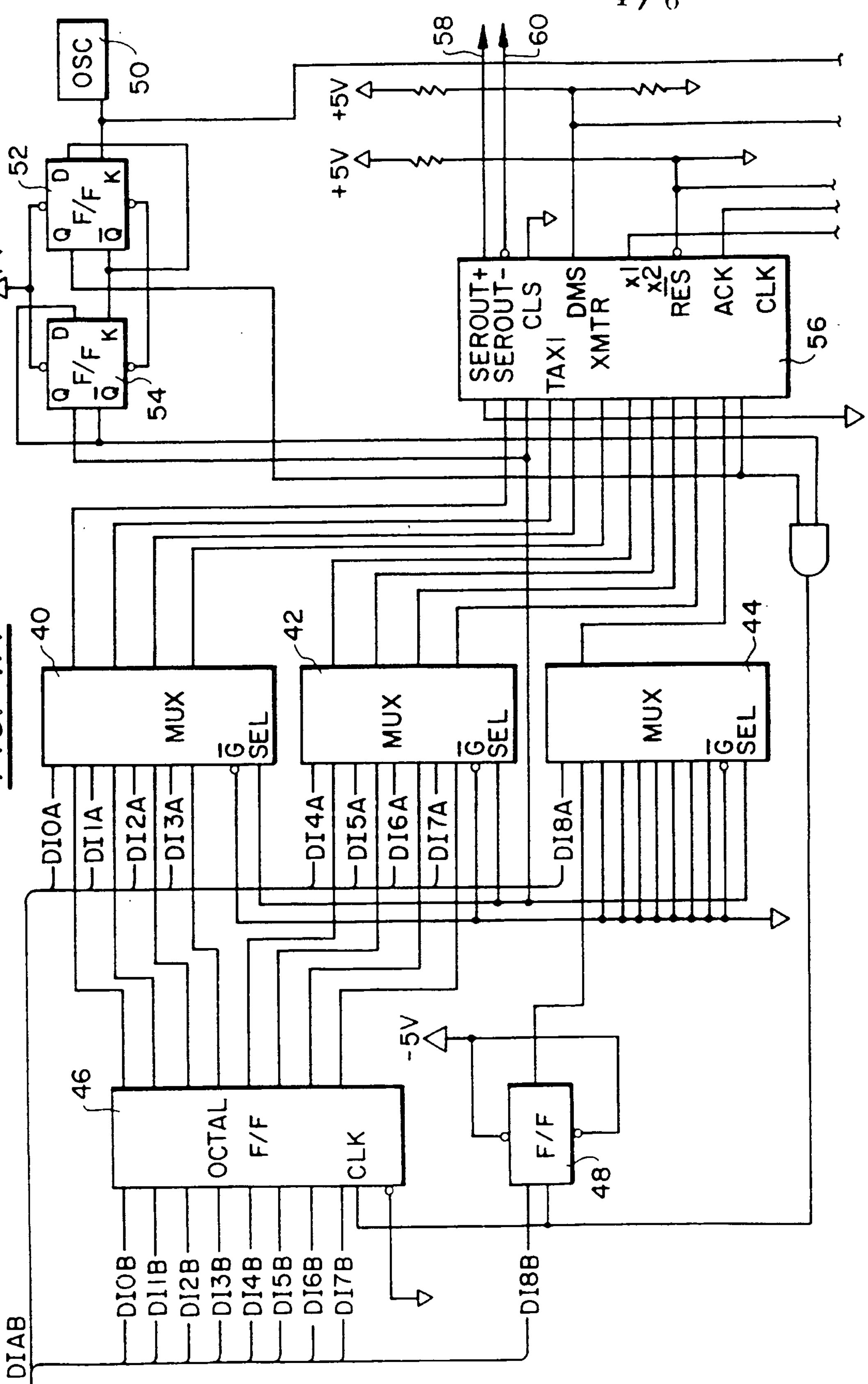

OSC
50
52
F/F
D
K
Q
+V
54
58
60
+5V
+5V
SEROUT+
SEROUT-
CLS
DMS
x1
x2
RES
ACK
CLK
TAXI
XMTR
56
40
MUX
G
SEL
42
44
DI0A
DI1A
DI2A
DI3A
DI4A
DI5A
DI6A
DI7A
DI8A
46
OCTAL
F/F
CLK
-5V
48
DI0B
DI1B
DI2B
DI3B
DI4B
DI5B
DI6B
DI7B
DI8B
DIAB

FIG. 4A

FIG. 4B

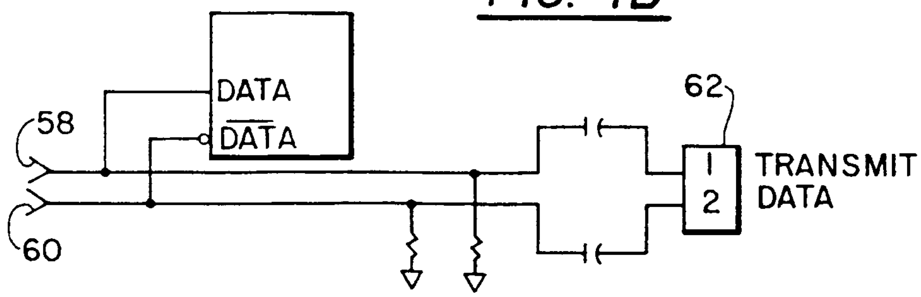
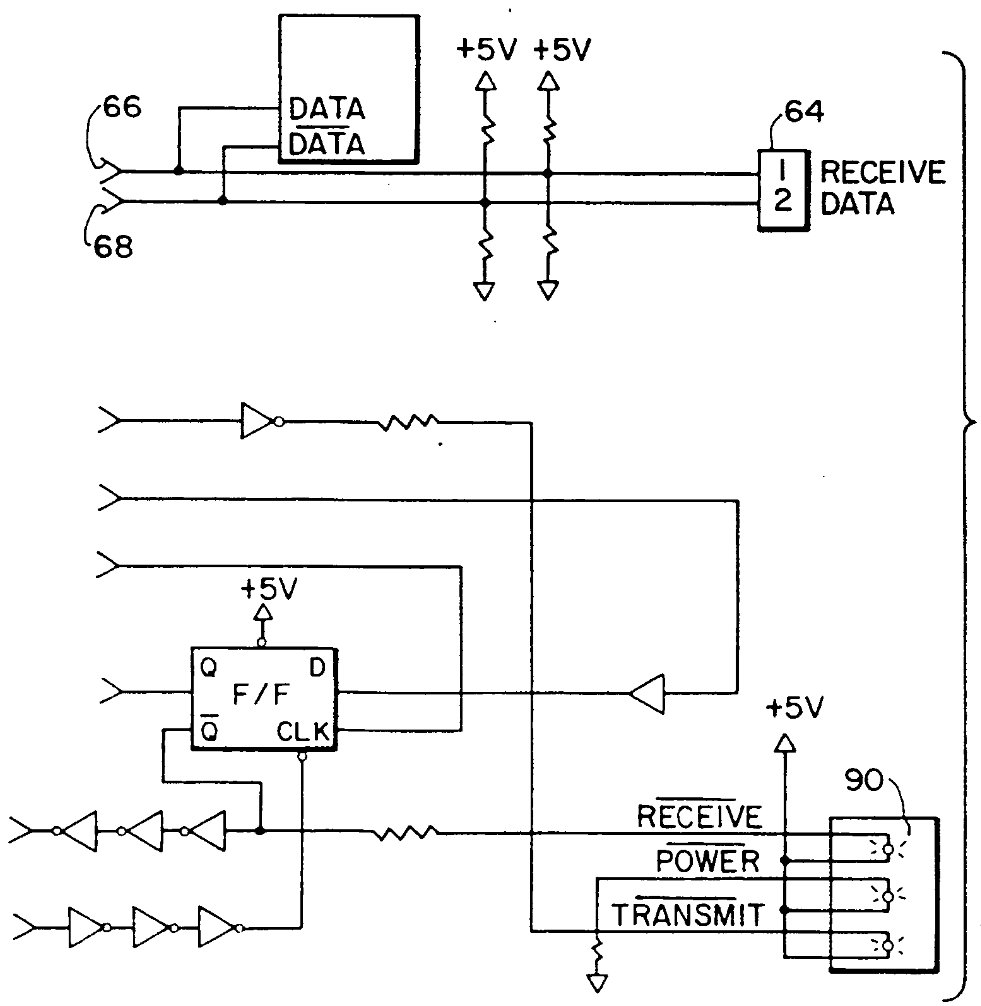

DATA
DATA
58
60
62
1
2
TRANSMIT
DATA

FIG. 5B


+5V
+5V
DATA
DATA
66
68
64
1
2
RECEIVE
DATA
+5V
Q
D
F/F
Q
CLK
+5V
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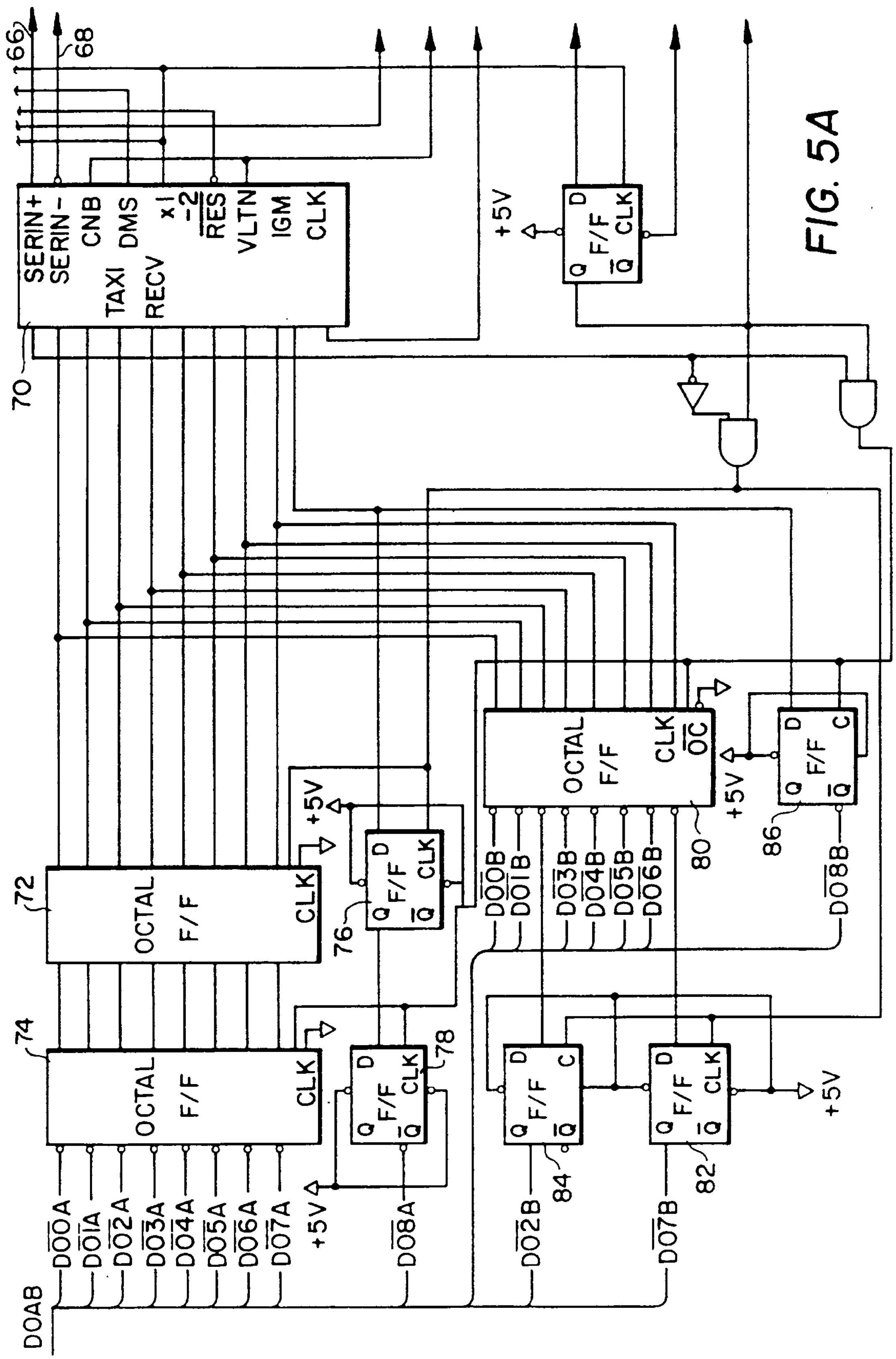
RECEIVE
POWER
TRANSMIT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SERIN-
CNB
DMS
x1
-2
RES
VLTN
IGM
CLK
TAXI
RECV
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CLK
Q
70
72
OCTAL
F/F
CLK
74
76
78
80
82
84
86
OC
DOAB
D00A
D01A
D02A
D03A
D04A
D05A
D06A
D07A
D08A
D00B
D01B
D02B
D03B
D04B
D05B
D06B
D07B
D08B
66
68

FIG. 5A

INTERNATIONAL SEARCH REPORT

PCT/US92/09521

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :G06F 3/00,13/00,5/00
US CL :395/275,500,800
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. :

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
APS US FILE TEXT SEARCH, REPORT ATTACHED

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,E	US,A, 5,206,946 (BRUNK) 27 APRIL 1993 See figure 2; col. 7, lines 4-49; col. 8, lines 1-49	1-8
Y	US,A, 4,276,656 (PETRYK, JR.) 30 JUNE 1981 See figure 3	1,7
Y	US,A, 4,908,823 (HAAGENS ET AL) 13 MARCH 1990 See figure 1	1,7
A	US,A, 4,939,735 (FREDERICS ET AL) 03 JULY 1990 See figure 1	1,7

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be part of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 JUNE 1993	13 JUL 1993

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	MENG-AI T. AN
Facsimile No. NOT APPLICABLE	Telephone No. (703) 305-9678

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/09521

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 4,866.609 (CALTA ET AL) 12 SEPTEMBER 1989 See figure 1-3	1,7
Y	US,A, 4,809,217 (FLORO ET AL) 28 FEBRUARY 1989 See figure 2	1-2 and 7-8